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(54) Circuit for producing pulse signals with a desired duty cycle

(57) An integrated circuit has a first circuit which receives an input signal and outputs a first output signal, wherein the first output signal is produced by changing the pulse width of the input signal, a second circuit which receives the first output signal and outputs a second output signal, wherein the second output signal is produced by delaying the first output signal and a control circuit. The control circuit has a first control circuit which receives the first and second output signals and controls the first circuit based on the first and second output signals and a second control circuit which receives the first and second output signals and controls the second circuit based on the first and second output signals.

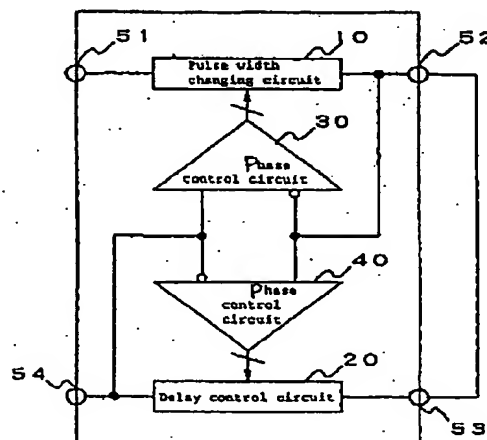


Fig. 1

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Description

[0001] The present invention relates to an integrated circuit and more particularly to an integrated circuit for producing pulse signals with a desired duty.

[0002] A conventional circuit of this type includes a pulse signal generating circuit. JP-A-60-217722 discloses a conventional integrated circuit which has the signal generating circuit (hereinafter referred to as a first conventional integrated circuit).

[0003] Referring to Fig. 12, the first conventional integrated circuit has a delay path L0 with a delay time of $t_1 + t_2$. Delay path L0 consists of a series connection of a delay path L1, with a delay time of t_1 , and a delay path L2, with a delay time of t_2 . The output of delay path L0 is logically inverted by an inverter 1202 and fed back into the input of delay path L0 through an OR circuit 1201. The output from the middle tap point of delay path L0, the output of delay path L1, is also logically inverted by an inverter 1203 and fed back into the input of delay path L0 through an OR circuit 1201. Thus, a delay loop with a delay time of t_1 and a delay loop with a delay time of $t_1 + t_2$ are formed.

[0004] Next, the operation of the first conventional integrated circuit will be described.

[0005] As described above, logic signals (pulse signals) circulating through the two delay loops are integrated into one logic signal by OR circuit 1201, which is then returned to the input of delay path L0. In other words, signals, which circulate two types of delay loops having different delay times, interfere with each other, and the generated pulse signal is outputted. As a result, by maneuvering the two delay times t_1 and t_2 , the duty of the output pulse signal, the ratio of $t_m = t_1$ and $t_m = t_1 + t_2$, is controlled to produce a desired duty.

[0006] Another conventional integrated circuit is disclosed in JP-A-63-237610 (hereinafter referred to as a second conventional integrated circuit).

[0007] Referring to Fig. 14, the second conventional integrated circuit comprises: an exclusive OR circuit 1401 which produces a multiplied signal by performing an exclusive OR operation on the input signal and the input signal delayed by a plurality of delay circuits 1402, each of which has a different delay time; a duty determination circuit 1403 for outputting the determination signal specifying the direction of change in delay amounts of the delay circuit 1402 for making the output of the exclusive OR circuit 1401 a fixed duty value; and a selector 1404 for inputting the determination signal from the duty determination circuit 1403 and switching the delay time of the delay circuit 1402 based on the specified direction of change in delay time.

[0008] In Fig. 15, duty determination circuit 1403 includes an integration circuit 14031 that is used for detecting the high and low level pulse widths of the output signal.

[0009] Next, the operation of the second conventional integrated circuit will be described.

[0010] Duty determination circuit 1403 detects the high and low level pulse widths of the multiplied signal outputted from the exclusive OR circuit as a voltage, and switches selector 1404 so that the high and low level pulse widths become the predetermined value. Thus, the duty of the output signal produced by multiplying the input signal can be set to a desired value.

[0011] In the first conventional integrated circuit, however, a problem occurs because the lower limit of the operating frequency is restricted. If the delay time of the delay path is increased, the waveform of the pulse signal deteriorates because the circuit is configured as a ring oscillator. The waveform deterioration produces noise which causes a malfunction.

[0012] The first conventional integrated circuit also produces another problem because after the circuit operation stabilizes and stops for a time longer than the cycle of the input signal, the input signal can not be followed immediately when the input of the input signal is started again. This is because the circuit is configured as a ring oscillator.

[0013] On the other hand, in the second conventional integrated circuit, a problem occurs because after the circuit operation stabilizes and stops for a time longer than the cycle of the input signal, the input signal can not be followed immediately when the input of the input signal is started again. This is because integration circuit 14031 is used in the duty determination means.

[0014] The second conventional integrated circuit causes other problems because the output signal is restricted to the signal obtained by multiplying the input signal and the duty of the output signal does not become 50 percent unless the duty of the input signal is 50 percent.

[0015] Accordingly, an object of the present invention is to provide a integrated circuit which equalizes the high level pulse width of the output signal with the low level pulse width of the output signal even if the high and low level pulse widths in the input signal are different.

[0016] According to one aspect of the present invention, an integrated circuit is provided which comprises: a first circuit which receives an input signal and outputs a first output signal, wherein the first output signal is produced by changing the pulse width of the input signal; a second circuit which receives the first output signal and outputs a second output signal, wherein the second output signal is produced by delaying the first output signal; a first control circuit which receives the first and second output signal and controls the first circuit based on the first and second output signals; and a second control circuit which receives the first and second output signals and controls the second circuit based on the first and second output signals.

[0017] According to another aspect of the present invention, an integrated circuit is provided which comprises: a first circuit which receives an input signal, and outputs a first output signal which is increased in proportion to the high level width of the input signal to the

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low level width of the input signal when the high level width is less than the low level width, or in proportion to the low level width of the input signal to the high level width of the input signal when the low level width is less than the high level width; and a second circuit which inputs the first output signal and outputs a second output signal, wherein the first output signal is produced by delaying the output signal.

[0018] Other features and advantages of the invention will be made more apparent by the following detailed description and the accompanying drawings, wherein:

Fig. 1 is a block diagram of a first embodiment of the present invention;

Fig. 2 is a block diagram of pulse width changing circuit 10 of the present invention;

Fig. 3 is a waveform diagram showing the operation of pulse width changing circuit 10;

Fig. 4 is a block diagram of delay control circuit 20 in the present invention;

Fig. 5 is a block diagram of delay selection circuit 21 in the present invention;

Fig. 6 is a waveform diagram showing the operation of delay selection circuit 21;

Fig. 7 is a block diagram of phase control circuit 30 in the present invention;

Fig. 8 is a waveform diagram showing the operation of the present invention when the high level pulse width of the input signal is less than the low level pulse width of the input signal;

Fig. 9 is a waveform diagram showing the operation of the present invention when the low level pulse width of the input signal is less than the high level pulse width of the input signal;

Fig. 10 is a block diagram of a second embodiment of the present invention;

Fig. 11 is a block diagram of a third embodiment of the present invention;

Fig. 12 is a block diagram of a first conventional integrated circuit;

Fig. 13 is a waveform diagram showing the operation of the first conventional integrated circuit;

Fig. 14 is a block diagram of a second conventional integrated circuit; and

Fig. 15 is a block diagram of duty determination circuit 1403 used in the second conventional integrated circuit.

[0019] In the drawings, the same reference numerals represent the same structural elements.

[0020] A first embodiment of the present invention will be described in detail below.

[0021] Referring to Fig. 1, a integrated circuit comprises: a pulse width changing circuit 10 which receives an input signal and changes the pulse width of the input signal; a delay control circuit 20 which delays the input signal for an optional delay time; and phase control circuits 30 and 40 which control pulse width changing circuit 10 and delay control circuit 20, respectively.

circuit 10 and delay control circuit 20, respectively.

[0022] Pulse width changing circuit 10 has an input terminal, an output terminal, and a control input terminal. The output terminal of pulse width changing circuit 10 is connected to the input terminal of delay control circuit 20, to an inverse input terminal of phase control circuit 30 which detects the trailing edge of the output signal from pulse width changing circuit 10, and to an input terminal of phase control circuit 40 which detects the leading edge of the output signal from pulse width changing circuit 10.

[0023] Delay control circuit 20 has an input terminal, an output terminal, and a control input terminal. The output of delay control circuit 20 is connected to an input terminal of phase control circuit 30 which detects the leading edge of the output signal from delay control circuit 20, and to an inverse input terminal of phase control circuit 40 which detects the trailing edge of the output signal from delay control circuit 20.

[0024] The control output of phase control circuit 30 is connected to the control input of pulse width changing circuit 10. The control output of phase control circuit 40 is connected to the control input of delay control circuit 20. Fig. 1 shows a typical configuration of this embodiment. Other similar configurations, which are not shown, are also intended to be covered by this embodiment.

[0025] Phase control circuit 30 has a terminal which receives the falling edge of an output signal from pulse width changing circuit 10 and a terminal which receives the rising edge of an output signal from delay control circuit 20. Phase control circuit 30 reduces the phase difference between the falling edge of the output signal from pulse width changing circuit 10 and the rising edge of the output signal from delay control circuit 20.

[0026] Phase control circuit 40 has a terminal which receives the rising edge of an output signal from pulse width changing circuit 10 and a terminal which receives the falling edge of an output signal from delay control circuit 20. Phase control circuit 40 reduces the phase difference between the rising edge of the output signal from pulse width changing circuit 10 and the falling edge of the output signal from delay control circuit 20.

[0027] Referring to Fig. 2, pulse width changing circuit 10 comprises: a variable delay circuit 11 which arbitrarily delays the input signal received at an input terminal 51 and outputs the output signal; an AND circuit 12 which performs an AND operation on the input signal received at input terminal 51 and the output signal from variable delay circuit 11; an OR circuit 13 which performs an OR operation on the input signal received at input terminal 51 and the output signal from variable delay circuit 11; and a selector 14 which receives the output signals of AND circuit 12 and OR circuit 13, and selectively outputs either one of the output signals to an output terminal 52. The delay time of variable delay circuit 11 can be set by a part of the control output from phase control circuit 30 via a terminal 55, which is a part of the control

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input. AND circuit 12 outputs an output signal s2 whose high level pulse width is narrowed by the delay time of variable delay circuit 11 by performing an AND operation on the input signal received at input terminal 51 and a signal s1 delayed by variable delay circuit 11. OR circuit 13 outputs an output signal s3 whose high level pulse width is widened by the delay time of variable delay circuit 11 by performing an OR operation on the input signal received at input terminal 51 and signal s1 delayed by variable delay circuit 11. Selector 14 is controlled by a part of the control output from phase control circuit 30 via a terminal s4, and outputs either output signal s2 from AND circuit 12 or output signal s3 from OR circuit 13 to output terminal 52.

[0028] Referring to Fig. 3, in pulse width changing circuit 10, by adjusting the delay time of variable delay circuit 11 and switching selector 14 by the control output from phase control circuit 30, the pulse width of the output signal, which is output from the output terminal 52, can be optionally changed.

[0029] Referring to Fig. 4, delay control circuit 20 comprises a plurality of delay selection circuits 21 connected in series. Delay control circuit 20 delays an input signal based on the control output from phase control circuit 40. Each of the delay selection circuits 21 selectively delay the input signal or output the input signal as is. In this embodiment, three delay selection circuits 21a, 21b and 21c are connected in series. More specifically, the delay time, by which delay control circuit 20 delays the input signal, can be set delicately by making the delay time of delay selection circuit 21b twice as long as delay selection circuit 21a, by making the delay time of delay selection circuit 21c twice as long as delay selection circuit 21b, and by individually controlling each of delay selection circuits 21a to 21c by the control output from phase control circuit 40 via terminals s6, s7 and s8, respectively. The number of delay selection circuits 21 and their delay times are not limited to those shown in this embodiment, and can be determined optionally as required.

[0030] In Fig. 5, delay selection circuit 21 includes a delay element 22 and a selector 23. A signal received at an input terminal s9 is branched into two signals, one of which is inputted into selector 23 as is, and the other is inputted into delay element 22. An output signal s10 is delayed by delay element 22 and inputted into selector 23. By switching the selection signal at terminal s12, either one of the input signals from terminal s9 or the output signal from delay element 22 is selected and outputted to an output terminal s11 based on the selection signal at terminal s12.

[0031] Referring to Fig. 6, in the operation of the delay selection circuit 21, the input signal received at input terminal s9 is outputted as the output signal to output terminal s11 if the selection signal from terminal s12 is at a low level. The output signal s10 from delay element 22 is outputted as the output signal to output terminal s11 if the selection signal s12 is at a high level. Also, the

delay amount can be set based on the storage capacity of delay element 22.

[0032] In Fig. 7, each of the phase control circuits 30 and 40 include a phase comparison circuit 31 and an up-down counter circuit 32. Phase comparison circuit 31 receives the signals from terminal 33 for detecting the leading edge of the pulse signal and terminal 34 for detecting the trailing edge of the pulse signal and compares the phases of the leading edge from terminal 33 and trailing edge from terminal 34. Phase comparison circuit 31 outputs the phase leading signal s13 and the phase delay signal s14 to up-down counter circuit 32. Up-down counter circuit 32 counts up or down based on the phase leading signal s13 or the phase delay signal s14 outputted from the phase comparison circuit 31, and outputs the control signal to pulse width changing circuit 10 or delay control circuit 20. Thus, in phase control circuit 30, pulse width changing circuit 10 is controlled to minimize the phase difference of the input signal. In phase control circuit 40, delay control circuit 20 is controlled to minimize the phase difference of the input signal.

[0033] Next, the operation of this embodiment will be described.

[0034] Referring to Fig. 1, a pulse signal received at input terminal 51 is sent to pulse width changing circuit 10 and its pulse width is changed by pulse width changing circuit 10. Delay control circuit 20 receives the signal outputted from pulse width changing circuit 10 and outputs it to output terminal 54 after controlling the delay time. The outputs of pulse width changing circuit 10 and delay control circuit 20 are fed back to pulse width changing circuit 10 and delay control circuit 20 through phase control circuits 30 and 40.

[0035] Phase control circuit 30 controls pulse width changing circuit 10 based on the times when the levels of the output signal from pulse width changing circuit 10 and the output signal from delay control circuit 20 change. More specifically, phase control circuit 30 controls pulse width changing circuit 10 so that the level of the output signal from pulse width changing circuit 10 falls when the level of the output signal from delay control circuit 20 rises.

[0036] Phase control circuit 40 controls delay control circuit 20 based on the times when the levels of the output signal from pulse width changing circuit 10 and the output signal from delay control circuit 20 change. More specifically, phase control circuit 40 controls delay control circuit 20 so that the level of the output signal from pulse width changing circuit 10 rises when the level of the output signal from delay control circuit 20 falls. Thus, in terminals 52, 53, and 54, pulse signals with the same pulse width at high and low levels, which are 50 percent duty signals, can be produced.

[0037] In Figs. 8 and 9, the high level pulse width of the signal obtained from terminal 52 is equalized with the low level pulse width because phase control circuit 30 controls pulse width changing circuit 10 to minimize

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the phase difference of the input signals. The signal obtained from terminal 54 is delayed by a half cycle from the signal obtained from terminal 52 to produce a high level pulse width that is equal to the low level pulse width, because phase control circuit 40 controls delay control circuit 20 to minimize the phase difference of the input signals.

[0038] When there is no phase difference between the trailing edge of the signal obtained from terminal 52 and the leading edge of the signal obtained from terminal 54, and there is no phase difference between the leading edge of the signal obtained from terminal 52 and the trailing edge of the signal obtained from terminal 54, the following relations are established between a cycle T of the input signal received at input terminal 51, a high level pulse width tw of the signal from terminal 52, and a delay time td from delay control circuit 20:

$$T = tw + td$$

$$tw = td.$$

[0039] Since $T = tw + td = 2tw$,

$$tw = T/2.$$

[0040] Thus, a pulse signal of which pulse width tw is $1/2$ of the cycle T can be produced, that is, the duty is 50 percent of the input signal.

[0041] Next, a second embodiment of the present invention will be described below.

[0042] Referring to Fig. 10, an integrated circuit according to this embodiment comprises: a pulse width changing circuit 10 which changes the pulse width of an input signal; a delay control circuit 20 which delays the input signal at an optional delay time; phase control circuits 30 and 40 which control pulse width changing circuit 10 and delay control circuit 20, respectively; and a buffer circuit 60 which delays the output signal from pulse width changing circuit 10 for a predetermined time and sends the signal to delay control circuit 20. In this embodiment, all of the components and connections, except buffer circuit 60, are identical to the corresponding components of the first embodiment shown in Fig. 1.

[0043] By providing a buffer circuit 60 between the output of pulse width changing circuit 10 and the input of delay control circuit 20, the load on delay control circuit 20 is decreased, and the circuit size of delay control circuit 20 can be reduced. Therefore, the output signals with 50 percent duty can be distributed to many loads.

[0044] Next, a third embodiment of the present invention will be described below.

[0045] Referring to Fig. 11, an integrated circuit according to this embodiment comprises: a pulse width changing circuit 10 which changes the pulse width of an input signal; a delay control circuit 20 which delays the input signal at an optional delay time; phase control circuits 30 and 40 which control pulse width changing circuit

circuit 10 and delay control circuit 20, respectively; a buffer circuit 60 which delays the output signal from pulse width changing circuit 10 for a certain time and sends the signal to delay control circuit 20; and a phase locked loop (PLL) circuit 70 connected to the input terminal 51 of pulse width changing circuit 10. In this embodiment, pulse width changing circuit 10, delay control circuit 20, and phase control circuits 30 and 40 are identical to the corresponding components of the first embodiment shown in Fig. 1. Buffer circuit 60 is identical to buffer circuit 60 of the second embodiment shown in Fig. 10.

[0046] Since PLL circuit 70 is connected to the input terminal 51 of pulse width changing circuit 10, the input signal is inputted into pulse width changing circuit 10 after passing through PLL circuit 70. An input terminal 53 of delay control circuit 20 is connected to the feedback input of PLL circuit 70. By matching the phase of the feedback signal received from terminal 53, that is, the output signal of buffer circuit 60, with the phase of the input signal inputted into an input terminal 55 of PLL circuit 70, the skew due to the delay of pulse width changing circuit 10 and buffer circuit 60 can be minimized.

[0047] As described above, the high level pulse width of an output signal can be equalized with the low level pulse width even if the high level pulse width of an input signal differs from the low level pulse width. Phase control circuits detect the high level pulse width of the input signal and the low level pulse width, and feed back the results to adjust the pulse width of the input signal. Therefore, pulse signals with a duty of 50 percent can be produced.

[0048] While this invention has been described in conjunction with the preferred embodiments described above, it will now be possible for those skilled in the art to put this invention into practice using various other manners.

Claims

1. An integrated circuit comprising:

a first circuit which receives an input signal and outputs a first output signal, wherein said first output signal is produced by changing the pulse width of said input signal;

a second circuit which receives said first output signal and outputs a second output signal wherein said second output signal is produced by delaying said first output signal;

a first control circuit which receives said first and second output signals and controls said first circuit based on said first and second output signals; and

a second control circuit which receives said first and second output signals and controls said second circuit based on said first and second output signals.

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2. The integrated circuit as claimed in claim 1, wherein said first control circuit controls said first circuit based on times when levels of said first and second output signals change.
3. The circuit as claimed in claim 1 or 2, wherein said second control circuit controls said second circuit based on times when levels of said first and second output signals change.
4. The circuit as claimed in claim 1, 2 or 3, wherein said first control circuit controls said first circuit so that the level of said first output signal falls when the level of said second output signal rises.
5. The circuit as claimed in claim 1, 2, 3 or 4, wherein said second control circuit controls said second circuit so that the level of said first output signal rises when the level of said second output signal falls.
6. An integrated circuit comprising:
 - a first circuit which receives an input signal, and outputs a first output signal which is increased in proportion to a high level width of said input signal to a low level width of said input signal when said high level width is less than the low level width or in proportion to the low level width of said input signal to the high level width of said input signal when said low level width is less than the high level width; and
 - a second circuit which receives said first output signal and outputs a second output signal which is produced by delaying said output signal.
7. The integrated circuit as claimed in claim 6, further comprising: a first control circuit which receives said first output signal and a second output signal, and controls said first circuit based on the phases of said first output signal and second output signal.
8. The circuit as claimed in claim 6 or 7, further comprising: a second control circuit which receives said first output signal and a second output signal, and controls said second circuit based on the phases of said first output signal and second output signal.
9. The circuit as claimed in any one of claims 1 to 8, wherein said first control circuit has
 - a first terminal which receives a falling edge of said first output signal and a second terminal which receives a rising edge of said second output signal, and reduces a phase difference between said falling edge of said first output signal and said rising edge of said second output signal.
10. The circuit as claimed in any one of claims 1 to 9, wherein said second control circuit
 - has a first terminal which receives a rising edge of said first output signal and a second terminal which receives a falling edge of said second output signal, and reduces a phase difference between said rising edge of said first output signal and said falling edge of said second output signal.
11. The circuit as claimed in any one of claims 1 to 10, further comprising:
 - a buffer circuit which receives said first output signal and outputs a third output signal to said second circuit, wherein said third output signal is produced by delaying said first output signal by said buffer circuit.
12. The integrated circuit as claimed in claim 11, further comprising:
 - a phase locked loop circuit which receives said input signal and said third output signal, and outputs a fourth output signal to said first circuit so that a phase of said input signal adjusts a phase of said third output signal.

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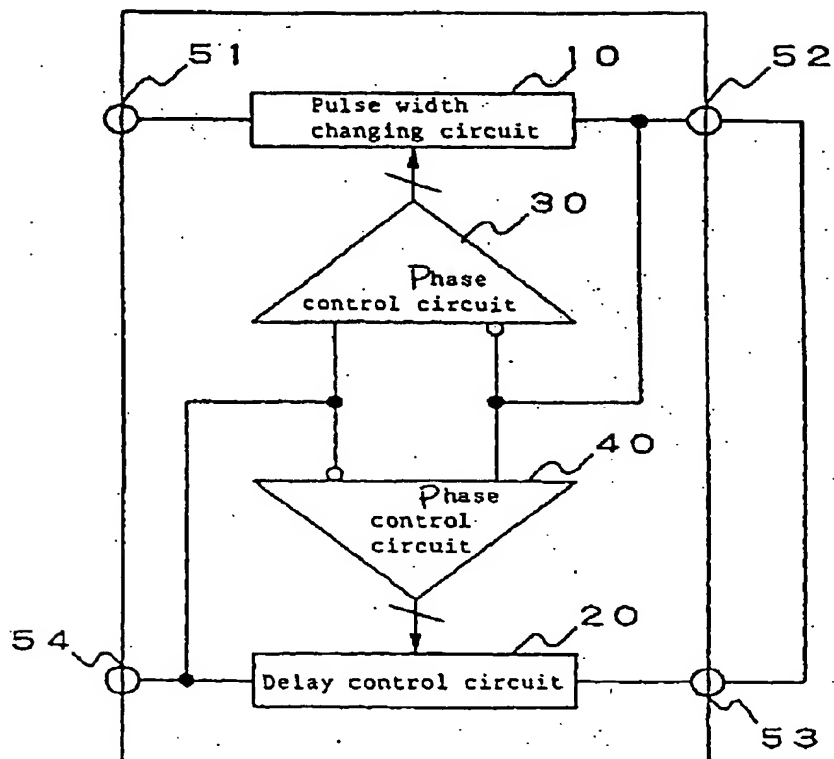


Fig. 1

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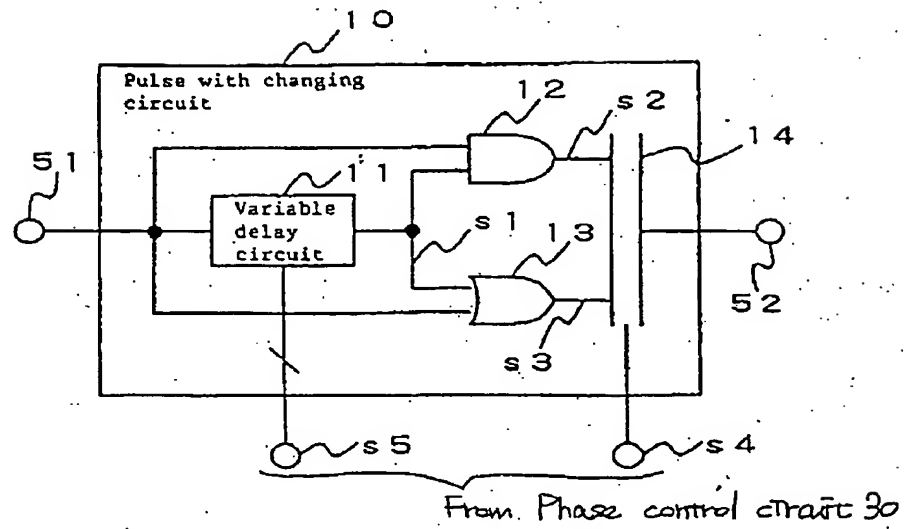


Fig. 2

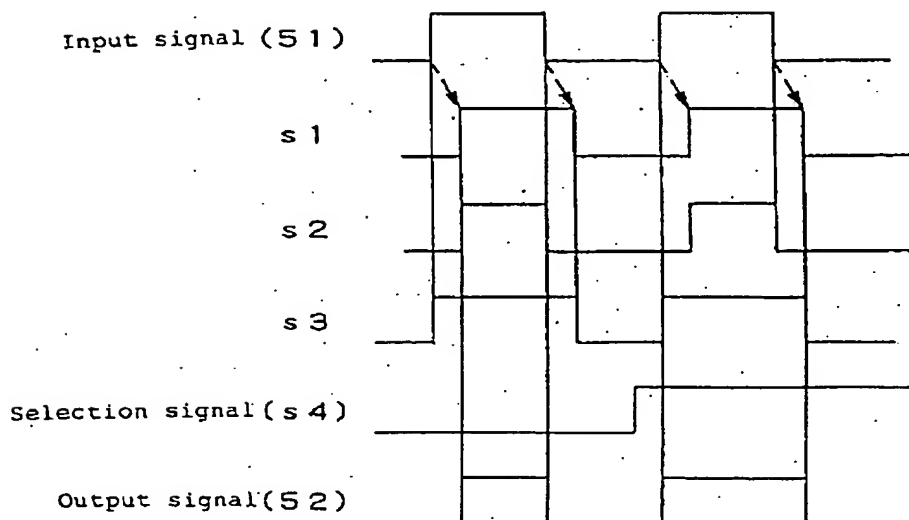
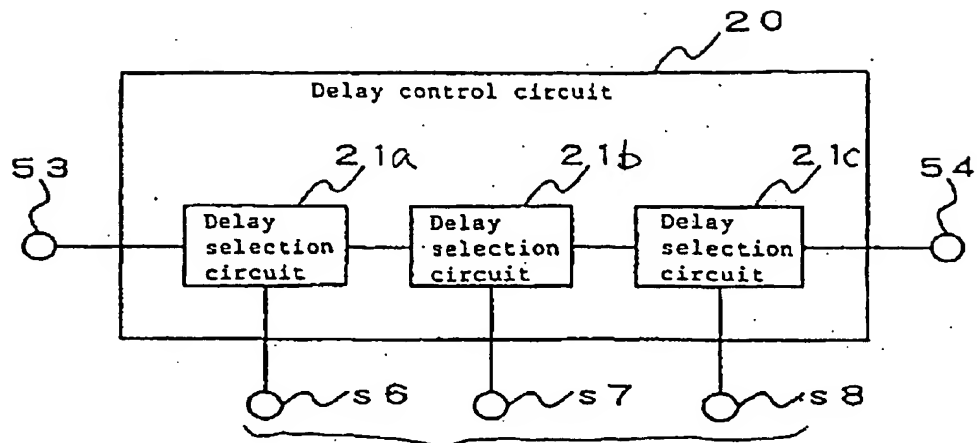


Fig. 3

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From Phase control circuit 40

Fig. 4

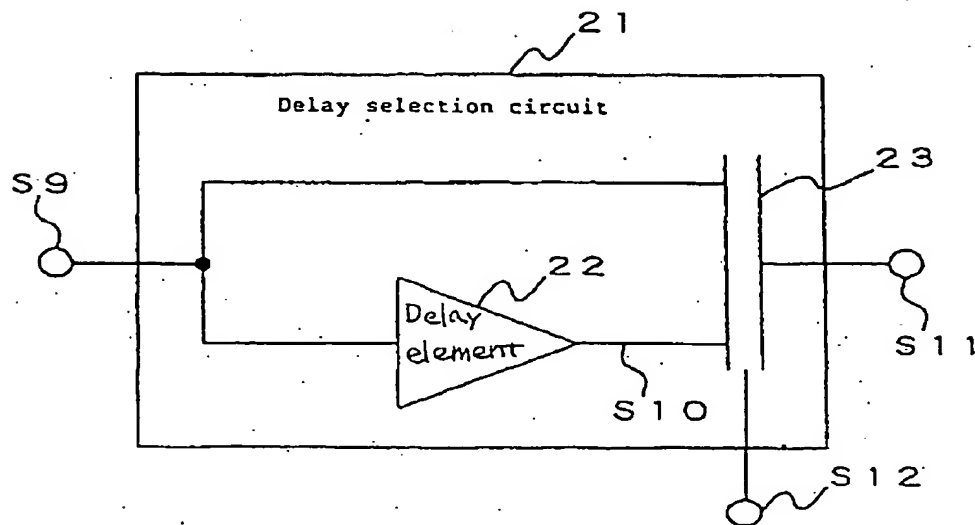


Fig. 5

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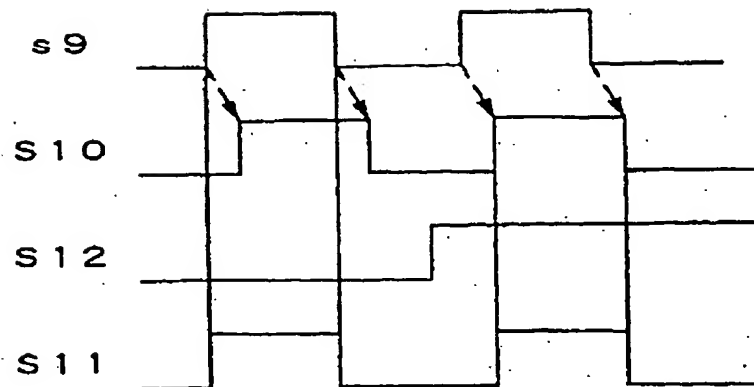


Fig. 6

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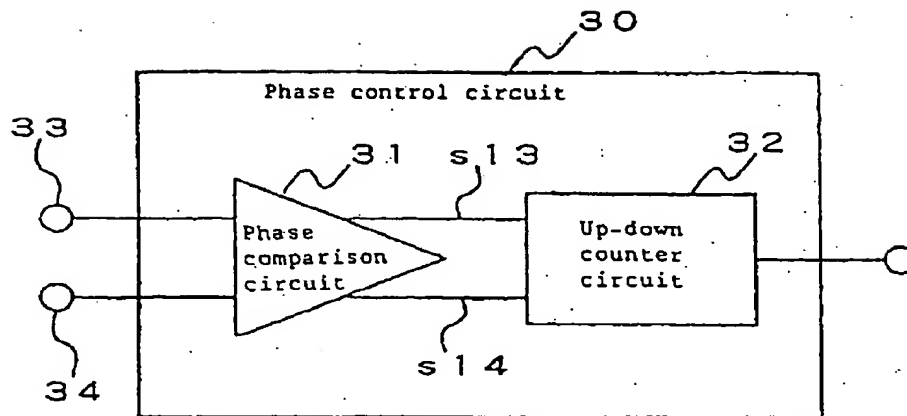


Fig. 7

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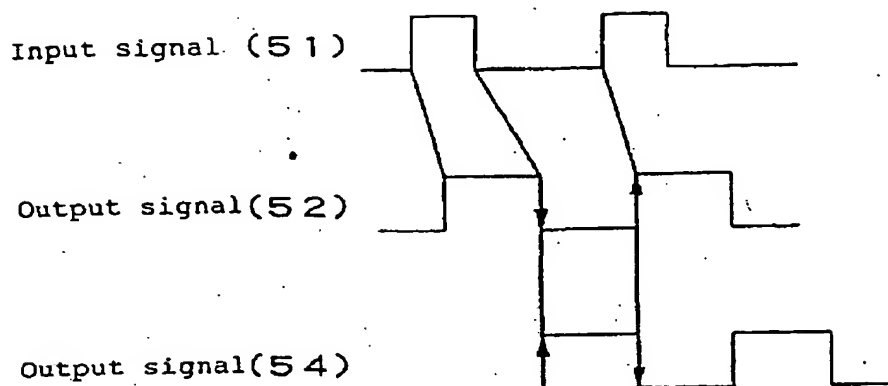


Fig. 8

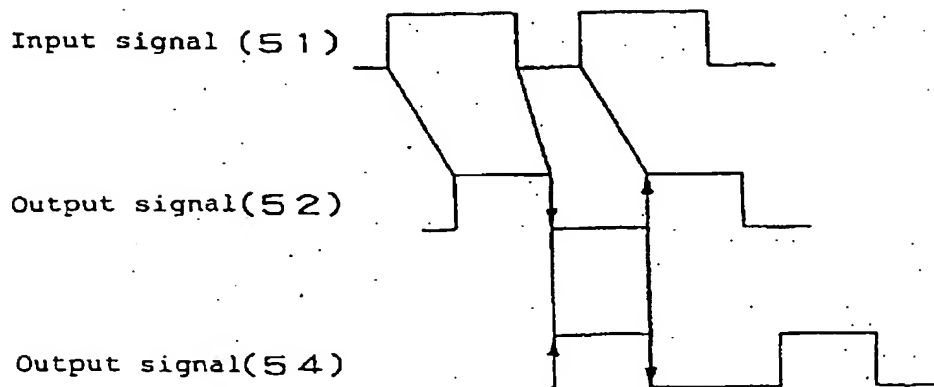


Fig. 9

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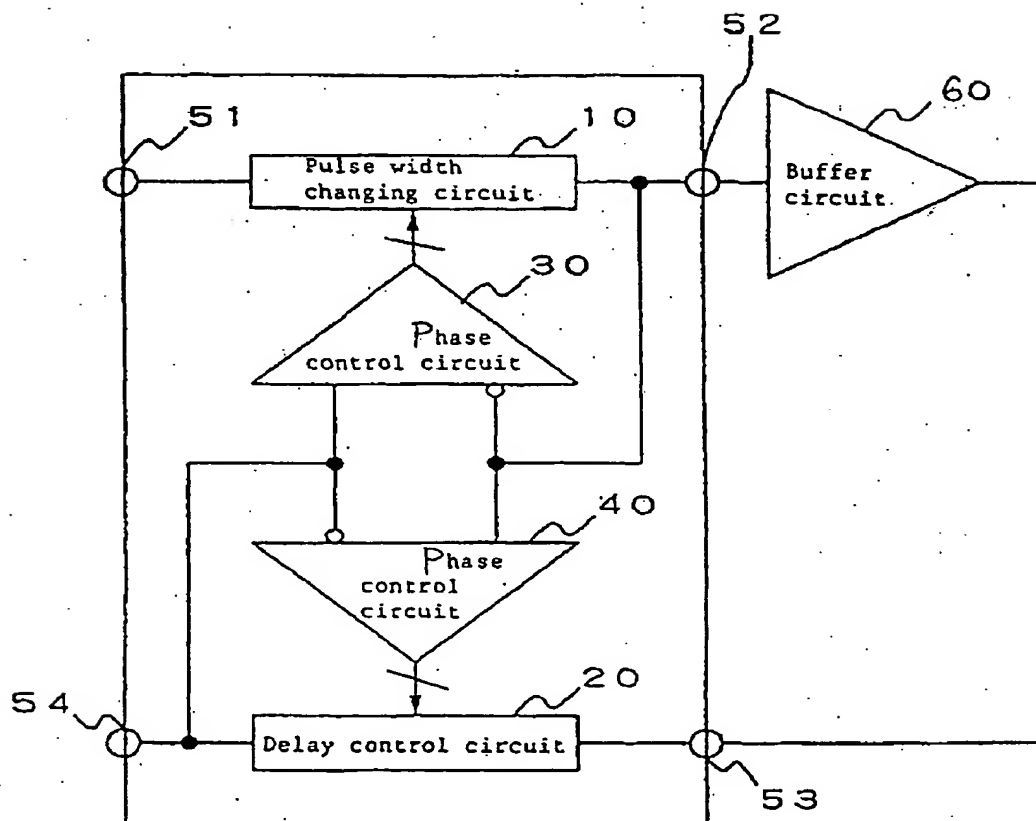


Fig. 10

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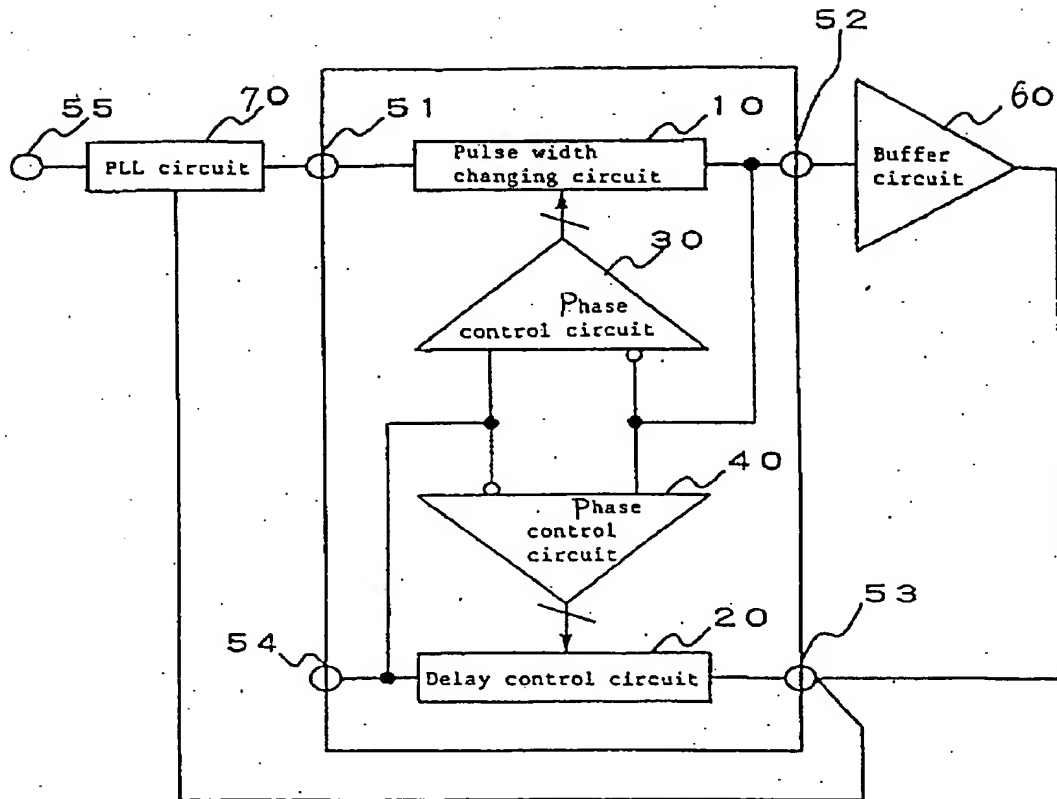


Fig. 11

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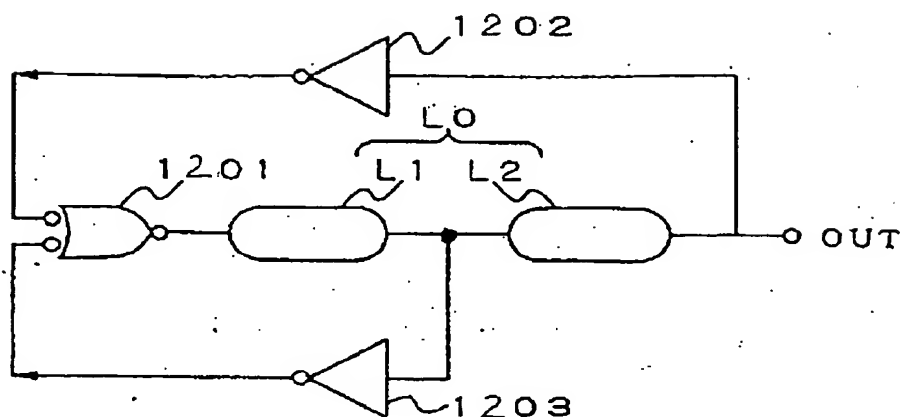


Fig. 12



Fig. 13

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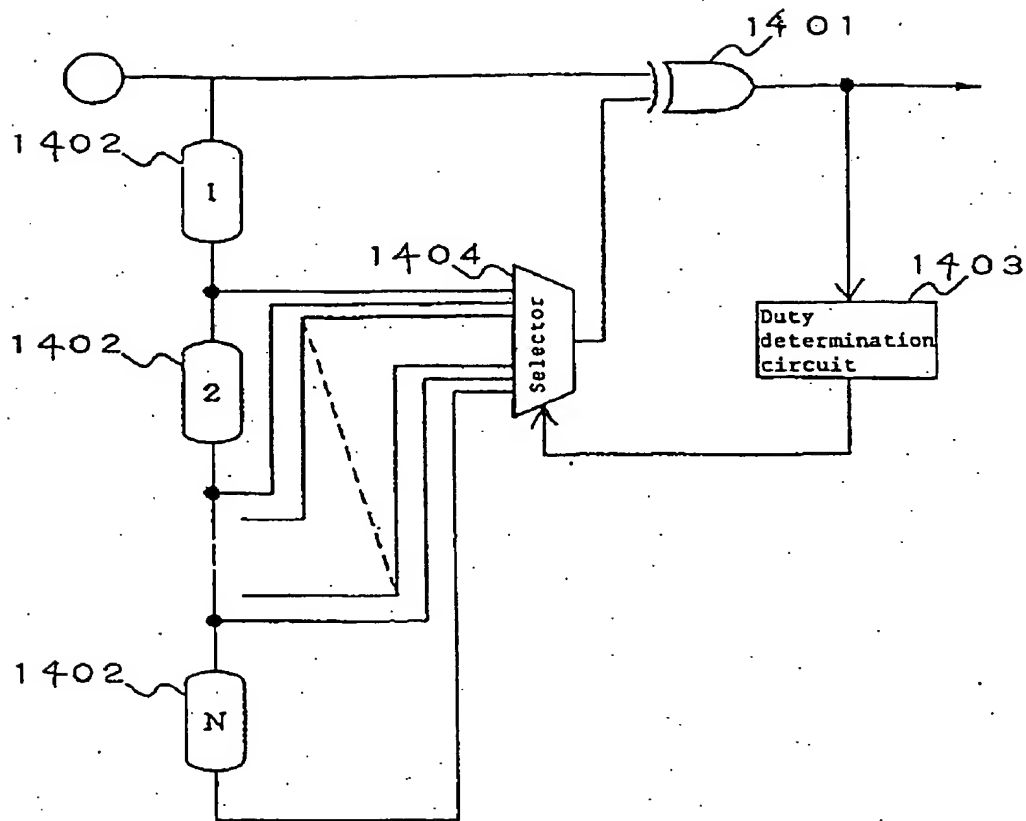


Fig. 14

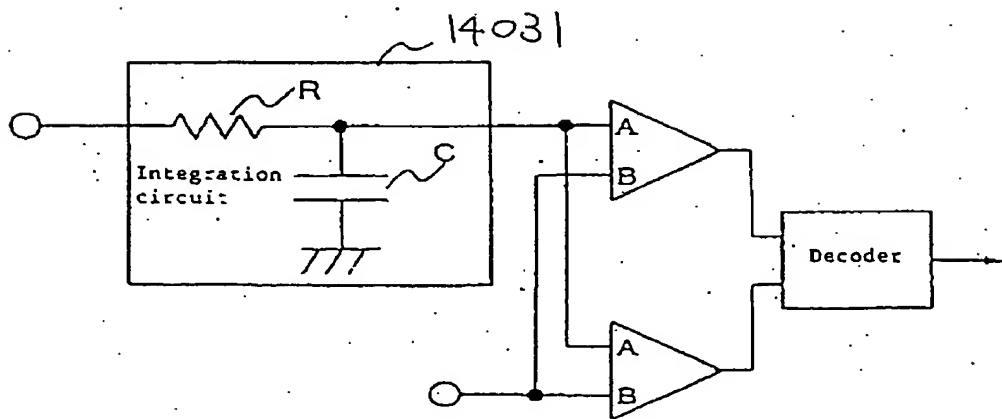


Fig. 15

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European Patent
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EUROPEAN SEARCH REPORT

Application Number
EP 99 10 0394

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	EP 0 762 262 A (MITSUBISHI ELECTRIC CORP) 12 March 1997 * column 11, line 30-45; figure 11 * * column 13, line 11-26; figure 18 *	1	H03K5/13 H03K3/017
A	US 5 670 903 A (MIZUNO MASAYUKI) 23 September 1997 * column 4, line 48 - column 6, line 20; figure 2 *	1	
A	US 5 105 108 A (NGO DUC) 14 Apr 11 1992 * column 3, line 67 - column 4, line 42; figure 3 *	1	
X	WO 95 22206 A (RAMBUS INC) 17 August 1995 * page 8, paragraph 3 - page 11, paragraph 1; figure 2 * * page 25, paragraph 3 - page 26, paragraph 2; figure 5A *	6	
X	EP 0 604 126 A (MOTOROLA INC) 29 June 1994 * column 3, line 20 - column 4, line 41; figure 2 *	6	TECHNICAL FIELDS SEARCHED (Int.Cl.6) H03K H03L
X	US 4 799 022 A (SKIERSZKAN SIMON J) 17 January 1989 * the whole document *	6	
The present search report has been drawn up for all claims			
Place of search MUNICH		Date of completion of the search 5 May 1999	Examiner Moll, P
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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 0762262 A	12-03-1997	JP 9074339 A	18-03-1997
		CN 1144926 A	12-03-1997
		US 5801559 A	01-09-1998
US 5670903 A	23-09-1997	JP 2561037 B	04-12-1996
		JP 8069339 A	12-03-1996
		DE 19531962 A	14-03-1996
US 5105108 A	14-04-1992	NONE	
WO 9522206 A	17-08-1995	AU 1841895 A	29-08-1995
		JP 9512966 T	22-12-1997
		US 5614855 A	25-03-1997
EP 0604126 A	29-06-1994	GB 2273834 A	29-06-1994
		SG 49826 A	15-06-1998
		US 5418485 A	23-05-1995
US 4799022 A	17-01-1989	CA 1254957 A	30-05-1989
		GB 2199457 A,B	06-07-1988
		JP 63204813 A	24-08-1988

EPO FORM P449

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82